N32G030x Series Errata Sheet V1.5.0

Contents

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1 Errata List

Table 1-1Errata overview

Errata link			Chip version	
			Version A	Version B
Section 2: PWR	Section 2.1: Power on after power off		●	-
	Section 2.2: Support for STOP+ mode		●	-
Section 3: RCC	Section 3.1: When running the program, the LSI is biased		●	●
	Section 3.2: LSE is affected by toggling of adjacent pins		●	●
	Section 3.3: HSE instability causes chips to run off		●	●
Section 4: GPIO and AFIO	Section 4.1: GPIO analog function		●	●
	Section 4.2: IO reverse current		●	●
Section 5: ADC	Section 5.1：When the injection channel is triggered, the regular channel is also triggered		●	●
	Section 5.2: ADC injection channel conversion		●	-
Section 6: SPI&I2S	Section 6.1 SPI	Section 6.1.1: SPI baud rate setting when CRC is enabled	●	●
		Section 6.1.2: Slave mode CRC check	●	●
		Section 6.1.3: When the power supply is 1.8V~2.0V, the SPI data rate may not reach 18Mbps	●	●
	Section 6.2：I2S	Section 6.2.1: PCM long frame mode	●	●
		Section 6.2.2: I2S master clock is not output	●	-
Section 7: I2C	Section 7.1: A software event that must be managed before the current byte is transferred		●	●
	Section 7.2: Attentions when reading a single byte at time		●	●
	Section 7.3: Using DMA concurrently with other peripherals		●	-
	Section 7.4: STOP establishment time exceeds minimum threshold in standard mode		●	●
Section 8: USART	Section 8.1: Parity error flag		●	●
	Section 8.2: RTS hardware flow control		●	●
Section 9: TIM	Section 9.1: TIM overcapture		●	●
	Section 9.2: ADTIM and GPTIM cannot generate compare events under certain circumstances		●	●

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	Section 9.3: The issue of switching from another mode to 100% or 0% duty cycle PWM mode	●	●
Section 10: LPTIM	Section 10.1: LPTIM COUNTMODE	●	-
Section 11: RTC	Section 11.1: RTC Timing	●	-
	Section 11.2: RTC subsecond match	●	●
	Section 11.3: RTC second match	●	●
	Section 11.4: RTC calendar function cannot be initialized multiple times within 1 second	●	●
	Section 11.5:The RTC triggers the TISOVF flag by mistake	●	●
	Section 11.6: RTC_DATA register lock	●	●

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2 PWR

2.1 Power on after power off

Description

When the power supply is powered off, the power is not completely powered down to about 1.6V and then powered on to the normal working voltage, the power-on may not be successful.

Resolution

When the MCU is powered off, it is necessary to ensure that the chip VDD voltage drops below 100mV, and then power on to the normal operating voltage.

2.2 Support for STOP+ mode

Description

Version A supports the STOP+ mode, while Version B has removed the STOP+ mode to address the rare issue of power-on failure caused by IO reverse current leakage prior to VDD power-on.

Solution

When configuring the STOP mode, the STOPPLUSEN bit should be disabled, and the PDSTOP bit should be selected to enter the STOP mode. There may be minor changes in power consumption (STOP power consumption meets the specified parameters in the data manual).

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3 RCC

3.1 When running the program, the LSI is biased

Description

When the LSI is running the program, the Jitter is large, the average frequency (1S time) is 30K±1KHz, and the instantaneous frequency is 20K~45KHz.

Resolution

For precise timing, it is recommended that customers use LSE instead of LSI.

3.2 LSE is affected by toggling of adjacent pins

Description

LSE is affected by toggling of adjacent pins.

Resolution

Avoid toggling of adjacent pins of LSE

3.3 HSE instability causes chips to run off

Description

When enabling HSE and waiting for the HSE ready flag to be set to run the code directly, the system program may be unstably due to the HSE clock, causing the program to run away.

Resolution

After enabling HSE, add a software delay of about 10 milliseconds, then wait for the HSE Ready flag to be set before running the code.

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4 GPIO and AFIO

4.1 GPIO analog function

Description

When the 4 GPIOs PA1/PA2/PA3/PA4 are in the high-level output state, when they switch to the analog function, there will be a short output voltage drop of about 30mv during the switching process.

Resolution

Avoid the above methods of use.

4.2 IO reverse current

Description

If the IO that does not support failsafe is powered on before VDD, an exception may occur at this time, and the external pin reset cannot return to normal after the exception.

Resolution

It is recommended that customers use the power-on of VDD prior to the power-on of IO.

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5 ADC

5.1 When the injection channel is triggered, the regular channel is also triggered

Description

The ADC converts continuously, and the external trigger of the regular channel is disabled. When the software or hardware trigger injection channel conversion, the regular channel may be converted, and the corresponding status bit of the regular channel conversion will be set.

Resolution

Ignore the status bit and data generated by the regular channel.

5.2 ADC injection channel conversion

Description

The injection channel conversion is triggered immediately after the regular channel conversion is completed, and the injection channel conversion cannot be completed.

Resolution

None

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6 SPI&I2S

6.1 SPI

6.1.1 SPI baud rate setting when CRC is enabled

Description

When the CRC check function is turned on, depending on the working environment of the SPI interface, such as board-level delay, ambient temperature, etc., both the SPI master and slave will have CRC check exceptions.

In the ideal room temperature environment of the laboratory, when the SPI clock is greater than 14MHz, an abnormal CRC check error may occur.

Resolution

When the CRC function is enabled, it is recommended that the CRC clock frequency configuration should not exceed 14MHz.

When a CRC exception error occurs, reduce the SPI baud rate configuration.

6.1.2 Slave mode CRC check

Description

SPI works in slave mode and CRC check has been enabled. Even if the NSS pin is high, as long as the SPI receives the clock signal, the CRC calculation will still be performed.

Resolution

Before using the CRC check, first clear the CRC data register so that the master and slave devices can keep the CRC check synchronously. The steps are as follows:

1. SPI enable bit reset (set to 0)
2. CRC check bit reset (set to 0)
3. CRC check bit set (set to 1)
4. SPI enable bit is set (set to 1)

6.1.3 When the power supply is 1.8V~2.0V, the SPI data rate may not reach 18Mbps

Description

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When the power supply is 1.8V~2.0V, the SPI data rate may not reach 18Mbps depending on the IO and board-level wiring delay characteristics.

The highest communication rate measured in the ideal environment of the laboratory is:

-25℃ ~45℃ can reach 18Mbps.

-40℃ ~-25℃, 45℃-105℃ : 12Mbps.

Resolution

If customers have 1.8V high temperature and low temperature SPI communication requirements, it is recommended to contact Nationstech Company for technical support.

6.2 I2S

6.2.1 PCM long frame mode

Description

When I2S works in master mode, PCM long frame mode, and the data format is "32bit" or "16bit extended to 32bit", the WS signal is one cycle per 16bit instead of 32bit.

Resolution

When I2S is the master mode and the long frame mode must be used, the 16bit data mode should be used.

6.2.2 I2S master clock is not output

Description

When I2S works in master mode, MCLK is enabled, and MCLK does not output after I2S transmission starts.

Resolution

None

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7 I2C

7.1 A software event that must be managed before the current byte is transferred.

Description

When EV7, EV7_1, EV6_1, EV6, EV2, EV8, and EV3 events occur, the events must be processed before the current byte is transferred, otherwise there may be a problem of reading an extra byte, reading duplicate data, or losing data. If the software does not read the N-1th byte before the stop signal is generated, the Nth byte in the shift register is corrupted (shifted one bit to the left).

Resolution

1. When using I2C to transfer more than one byte, try to use DMA mode
2. When using I2C interrupt, adjust the interrupt priority to the highest priority of the application
3. When the read data reaches the N-1th byte:
   a) Detect BSF as 1
   b) Configure SCL as GPIO open-drain output and set it to 0
   c) Set STOPGEN as 1
   d) Read the N-1th byte
   e) Configure SCL as I2C multiplexing function open-drain output mode
   f) read the last byte

7.2 Attentions when reading a single byte at time

Description

In the master read mode, when the length of the read byte is a single byte, a read data error may occur.

Resolution

When read single byte：

a) After receive ADDRF

b) Set ACKEN bit as 0

c) Clear ADDRF bit（Cleared by reading STS1 and then STS2）

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d) Set STOPGEN as 1

e) Read last byte。

7.3 Using DMA concurrently with other peripherals

Description

During I2C using DMA communication, if other peripherals are also using DMA, I2C communication will be abnormal.

Resolution

There are two workarounds:

1. During I2C using DMA communication, turn off other peripheral DMA.

2. When receive the penultimate byte, set the DMALAST bit of I2C->CTRL2

7.4 STOP establishment time exceeds minimum threshold in standard mode

Description:

In host mode: At a communication rate of 100K, triggering the slave's clock extension results in a STOP establishment time below 4μs.

Resolution:

It is recommended to reduce the communication rate to 50K or below, in accordance with the slave peripheral's timing requirements.

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8 USART

8.1 Parity error flag

Description

During the reception of one byte of data, before the stop bit is received, a parity error is detected, and the parity error flag is set. During this period, the parity error flag cannot be cleared by software (reading the status register and then reading the data register). If the parity error interrupt is enabled, the parity error interrupt handler will be entered multiple times.

Resolution

After the read data buffer flag is set, after receiving the data, the operation of clearing the parity error flag is performed. If the parity error interrupt is enabled, in order to avoid entering the interrupt processing function multiple times, when the parity error interrupt is entered for the first time, the parity error interrupt is turned off, and after the data is received, the parity error interrupt is turned on again.

8.2 RTS hardware flow control

Description

Enable RTS hardware flow control. When the USART receives data, the RTS signal will be automatically pulled high. If the byte data is not read from the data register in time, and a new byte is sent to the USART (violating the flow control protocol), the RTS signal will be pulled low again. USART waits again to receive the next frame of data.

Resolution

Before the next new data is received, the data is read out from the data register in time.

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9 TIM

9.1 TIM overcapture

Description

When reading the capture data register data (under normal circumstances, the read data register operation will cause the capture flag to be cleared), a trigger capture is generated externally, even if the previous capture has been correctly read and the new capture data is also is sent to the register exactly, but the overcapture flag is still detected. The system is critical for overcapture, but no capture data is lost.

Resolution

None

9.2 ADTIM and GPTIM cannot generate compare events under certain circumstances

Description

In edge-aligned mode, in up-counting PWM1 mode, when the current PWM cycle CCDATx shadow register >= AR value, the shadow register value of CCDATx in the next PWM cycle is 0. At the moment when the PWM cycle counter is 0, although the counter value = CCDATx shadow register value = 0 and OCxREF = 0, but still no compare event is generated.

Resolution

If it is not required that "the compare event is generated at the time when the counter value = CCDATx shadow register value =0", the compare event generated through another channel can replace the compare event that is not generated.

9.3 The issue of switching from another mode to 100% or 0% duty cycle PWM mode

Description

When switching from any mode (except frozen mode) to PWM1/2 mode, if the PWM duty cycle is set to 100% or 0%, the mode switch to PWM1/2 mode fail, if reconfig the PWM duty (not 0% or 100%), the mode switch to PWM1/2 mode success.

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Resolution

When switching from forced active/forced inactive/set channel x to the active level on match/ set channel x to the inactive level on match mode to PWM1/2 mode with a 100% or 0% duty cycle, modify CCxP to achive the PWM with 100% or 0% duty.

When switching from toggle mode to PWM1/2 mode with a 100% or 0% duty cycle, have no solution.

10 LPTIM

10.1 LPTIM COUNTMODE

Description

Configure the LPTIM clock source selection as the internal clock source timing, the counter mode is that when the counter increments according to each valid clock pulse on the LPTIM external Input1, the count value CNT can only count to ARR-1, and other configurations can count to ARR.

Resolution

None

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11 RTC

11.1 RTC Timing

Description

When the RTC is working, external reset/system reset will cause the clock provided by the HSE, LSE, and LSI to the RTC to be suspended, resulting in the suspension of the RTC counting.

Resolution

None

11.2 RTC subsecond match

Description

The RTC programmable alarm clock function does not enable matching of date, hour, minute and second, but only enables matching of sub-seconds (that is, an alarm interrupt is generated when sub-seconds match in every second). The alarm interrupt cannot be generated in the first sub-second match after the alarm function is enabled, and the alarm interrupt is generated for each sub-second match after that.

Resolution

None

11.3 RTC second match

Description

When the alarm clock configuration second matches, the chip enters the SLEEP mode. When the alarm interrupt is generated to wake up the chip from SLEEP, and the interrupt processing function is executed (only the operation of clearing the interrupt flag bit is performed), it immediately enters the STOP mode. The next alarm interrupt cannot wake the chip from STOP mode.

Resolution

Before setting the RTC time, you need to enter the RTC initialization mode. Before entering the RTC initialization mode, you need to wait for the value of the sub-second register to be less than the synchronous prescaler value and cannot be 0.

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11.4 RTC calendar function cannot be initialized multiple times within 1 second

Description

The RTC calendar function is initialized multiple times within 1 second, so that the RTC alarm clock interrupt cannot be generated.

Resolution

The interval between two initializations of the RTC calendar function is more than 1 second.

11.5 The RTC triggers the TISOVF flag by mistake

Description

When the system wakes up from STANDBY mode or the IWDG times out and the system reset, the RTC may triggers the TISOVF flag by mistake probability .

Resolution

Before entering STANDBY mode or IWDG time out, when the SHOPF flag is 0, configure RTC_SCTRL.SUBF[14:0] register for the first time, and SHOPF flag will set 1. When SHOPF flag is 0 again, configure RTC_SCTRL.SUBF[14:0] register for the second time. Note that NRST cannot be triggered during above process.

11.6 RTC_DATE register lock

Description

1. Before the system software reset, the RTC_DATE register is not read after reading the RTC_SUBS or RTC_TSH shadow register, and the RTC_DATE register will restores the default value after the system software resets and initializes the RTC without configuration or reads the RTC_DATE register;

2. When reading the calendar, after reading the RTC_SUBS or RTC_TSH shadow register, the value of the RTC_DATE register remains unchanged;

Resolution

1. Read the RTC_DATE register before initializing the RTC;

2. After reading the RTC_SUBS or RTC_TSH shadow register, read the RTC_DATE register;

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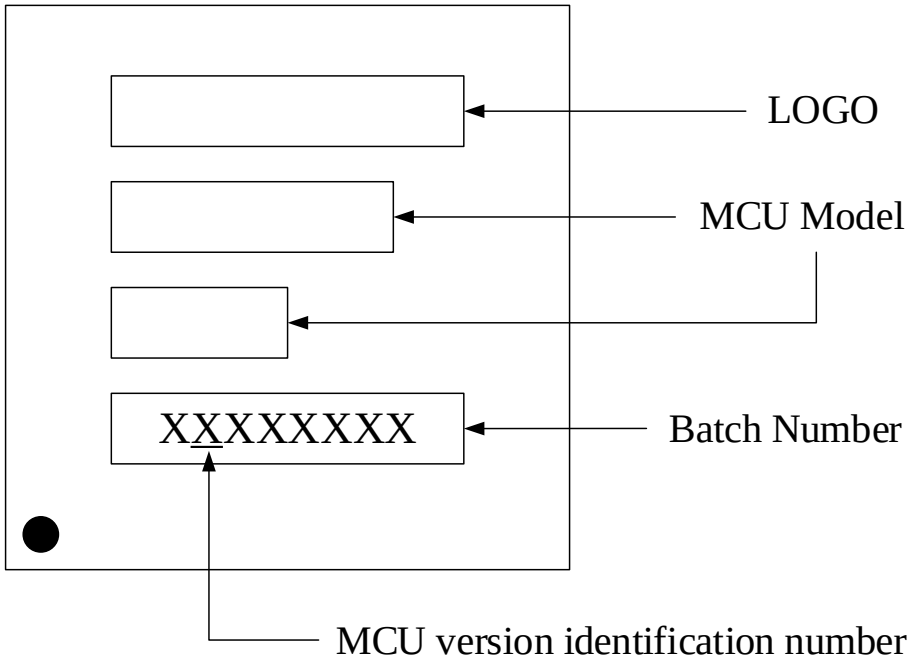

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13 Version history

Date	Version	Description
2022.3.18	V1.0	1. Initial version
2022.6.15	V1.1	1. Add section 9.2, ADTIM and GPTIM cannot generate compare events under certain circumstances 2. Modify section 3.1. Does not specify the specific value of the toggle frequency and pin. 3. Delete watermark, modify notice 4. Add section 11.4, RTC calendar function cannot be initialized multiple times within 1 second
2022.10.10	V1.2	1. Add section 3.1 2. Add section 6.1.3 3. Modify 6.1.1
2023.7.31	V1.3.0	1. Add section 3.3 2. Add section 11.5 3. Add section 11.6
2023.8.11	V1.4.0	1. Add section 2.2
2025.09.25	V1.5.0	1. Add Section 7.4 2. Add Section 9.3

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